Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec – 2017**

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| **Code :** | **14EC2034** | **Duration :** | **3hrs** |
| **Sub. Name :** | **FAULT TOLERANT TECHNIQUES** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | During wear-out phase the failure rate decreases (TRUE/FALSE). | CO1 | 1 |
| b. | Define MTBF. | CO1 | 2 |
| c. | Brief the relation between reliability and repair rate. | CO1 | 5 |
| d. | Write about the reliability analysis of series and parallel digital systems. | CO1 | 12 |
| (OR) | | | | |
| 2. | a. | Fault always causes circuit failure (TRUE/FALSE). | CO1 | 1 |
| b. | Narrate the “Stuck at” fault models with suitable example. | CO1 | 5 |
| c. | Analyze bridging fault with the help of a logic circuit. | CO1 | 5 |
| d. | Examine the random test generation method of combinational logic testing. | CO2 | 9 |
| 3. | a. | Appraise the principle of static redundancy in fault tolerant design of digital systems. | CO2 | 12 |
| b. | Interpret the test pattern generation using transition count testing for combinational logic. | CO2 | 8 |
| (OR) | | | | |
| 4. | a. | Narrate the fault tolerant design of digital systems using Sift-out Modular Redundancy. | CO3 | 10 |
| b. | Explain fault tolerant system design using error-correcting codes. | CO3 | 10 |
| 5. | a. | Illustrate the fault tolerant design of memory systems using Hamming Codes. | CO4 | 12 |
| b. | Summarize the working of the Fault Tolerant Multiprocessor. | CO4 | 8 |
| (OR) | | | | |
| 6. | a. | Examine the design process of the following practical fault tolerant systems.  i. SIFT ii. C.vmp | CO4 | 10 |
| b. | Assess the performance of 5MR reconfiguration scheme for the fault tolerant digital system design. | CO4 | 10 |
| 7. | a. | Define *fault-secure* and *self-testing* circuits. | CO5 | 4 |
| b. | Draw the model of a *totally self-checking* circuit and descript it. | CO5 | 4 |
| c. | Justify the effectiveness of totally self-checking algorithms for m-out-of-n codes. | CO5 | 12 |
| (OR) | | | | |
| 8. | a. | Describe controllability and observability for testable circuit design | CO6 | 6 |
| b. | Explain testable combinational logic circuit design using the Reed-Muller Expansion Technique. | CO6 | 14 |
|  | | **Compulsory:** |  |  |
| 9. |  | Highlight the design rules and advantages of Level-Sensitive Scan Design. Synthesize Double-latch and Single-latch testable circuits using LSSD. | CO6 | 20 |

ALL THE BEST